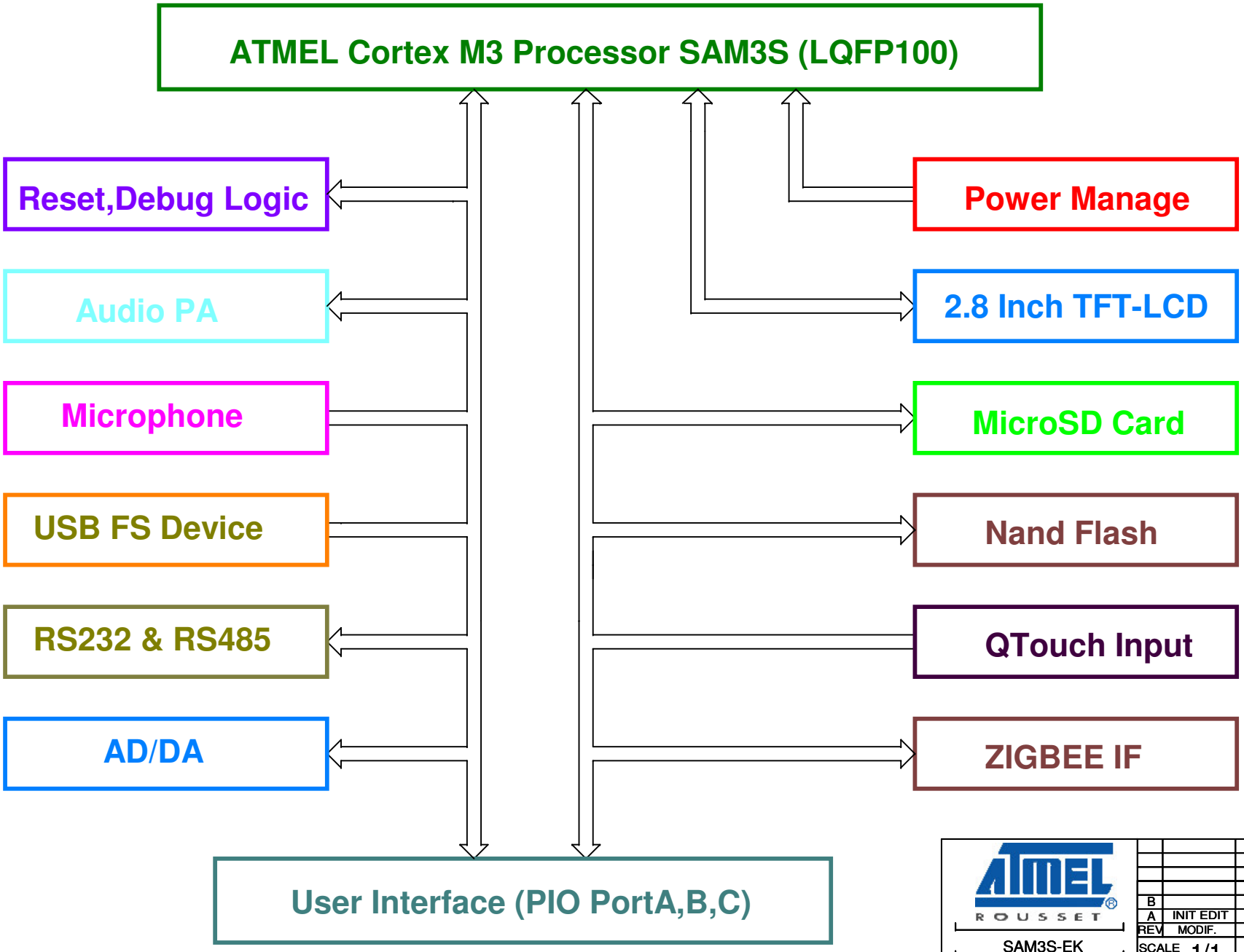
SAM3S-EK RevB Block Diagram



REV	MODIF.	DES.	DATE	VER.	DATE
B		PP	17-NOV-09		
A	INIT EDIT	NL	XX-XXX-XX	XXX	XX-XXX-XX

SAM3S-EK

Block Diagram

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REV. B

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REVISION HISTORY

REV	DATA	NOTE
A	2009.07	ORIGINAL RELEASED
B	2009.11	UPDATED

TABLE OF CONTENTS

SCHEMATICS CONVENTIONS

(1) Resistance Unit: "K" is "Kohm", "R" is "Ohm¸"
(2) "DNP" means the component is not populated by default

TEST POINT

PAGE	REFERENCE	FUNCTION
3	TP1, TP2, TP3, TP4	GND
4	TP5 TP6	UART TXD UART RXD
5	TP7 TP8, TP9	LCD backlight driver anode Aux ADC input for TSC
6	TP12	Optional audio PA input

JUMPER and SOLDERDROP

PAGE	REFERENCE	DEFAULT	FUNCTION
3	JP1	OPEN	Close to select JTAG boundary scan
	JP2	1-2	Analog reference voltage selection between 3.3V and 2.5V
	JP3	OPEN	Close to reinitialize the Flash contents and some of its NVM bits
	JP4	OPEN	Close for manufacturing test or fast programming mode
	JP5, JP6, JP7, JP8	CLOSE	Access for current measurement on each power rail
4	JP9	CLOSE	Nand Flash chip select enable
	JP11	CLOSE	RS485 bus termination enable
	JP10, JP12	OPEN	RS485 pull resistor selectors
5	JP13	CLOSE	LCD chip select enable
6	JP14, JP15	OPEN	Sync close to degrade gain stage on microphone input
	JP17, JP19	OPEN	Close to mux RIN/LIN into MONO-IN path within audio PA
	JP16, JP21	OPEN	Close for impedance matching on AD/DA BNC port
	JP18	1-2	ADC input selection between BNC port and potentiometer
	JP20	OPEN	Close to fix in mono speaker mode, no matter stereo plug state
	SD1	OPEN	DAC path isolation on sharing channel
	SD2	CLOSE	Lead PB13 as AUDIO_OUTL channel
7	JP22, JP23, JP24	1-2	DC voltage selection between 3.3V and 5V on PIO expansion ports
	JP25	CLOSE	Button BP2 disable
	JP26	CLOSE	Button BP3 disable
	JP27	CLOSE	Power consumption measure for ZigBEE module

PIO MUXING

PIOA	USAGE	PIOA	USAGE	PIOB	USAGE	PIOC	USAGE	PIOC	USAGE
PA0	TSLIDR_SL_SNS	PA16	TSC_IRQ/ZB_IRQ0	PB0	MIC INPUT	PC0	D0	PC16	NAND_ALE
PA1	TSLIDR_SL_SNSK	PA17	TSC_BUSY/ZB_IRQ1	PB1	ANA INPUT	PC1	D1	PC17	NAND_CLE
PA2	TSLIDR_SM_SNS	PA18	ZB_RSTN	PB2	ZB_NPCS2	PC2	D2	PC18	NAND_RDYBSY
PA3	TSLIDR_SM_SNSK	PA19	LED_BLUE	PB3	USER_PB1	PC3	D3	PC19	REGSEL_LCD
PA4	TSLIDR_SR_SNS	PA20	LED_GREEN	PB4	JTAG	PC4	D4	PC20	LED_RED(POWER)
PA5	TSLIDR_SR_SNSK	PA21	RXD1	PB5	JTAG	PC5	D5	PC21	USB_CNX
PA6	MCI_CD	PA22	TXD1	PB6	JTAG	PC6	D6	PC22	TVALID_SNS
PA7	CLK_32K	PA23	COM1EN	PB7	JTAG	PC7	D7	PC23	TVALID_SNSK
PA8	CLK_32K	PA24	RTS1	PB8	CLK_12M	PC8	WR_LCD	PC24	TUP_SNS
PA9	RX_UART0	PA25	CTS1	PB9	CLK_12M	PC9	NAND_OE	PC25	TUP_SNSK
PA10	TX_UART0	PA26	MCI	PB10	USB_DDM	PC10	NAND_WE	PC26	TDWN_SNS
PA11	TSC_CS	PA27	MCI	PB11	USB_DDP	PC11	RD_LCD	PC27	TDWN_SNSK
PA12	MISO	PA28	MCI	PB12	ERASE	PC12	USER_PB2	PC28	TLEFT_SNS
PA13	MOSI	PA29	MCI	PB13	AUDIO OUT R	PC13	EN_LCD	PC29	TLEFT_SNSK
PA14	SPCK	PA30	MCI	PB14	AUDIO OUT L	PC14	NAND_NCS0	PC30	TRIGHT_SNS
PA15	ZB_SLPTR	PA31	MCI			PC15	NSC1_LCD	PC31	TRIGHT_SNSK

DEFAULT NO POPULATE PARTS

PAGE	REFERENCE	FUNCTION
3	J1, R1	External clock resource input
	Y1, R3, R7	Backup 12MHz crystal
	R6, R8	Isolation between 12MHz clock source and GPIO line
	R9, R10	Isolation between 32KHz clock source and GPIO line
4	R22	Optional write protection on NAND flash
	R23	Optional pull up for open drain output on equivalent device
	R24, R30	Differential impedance matching for RS485 cable
	R25	Disconnect RS485 Receive data from PA21
5	D1	Optional ESD protection for LCD touch panel
	R61, R62, RA2, RA3	Optional databus termination for LCD controller

ATMEL ROUSSET

REV	MODIF.	DES.	DATE	VER.	DATE
B		PP	17-NOV-09		
A	INIT EDIT	NL	XX-XXX-XX	XXX	XX-XXX-XX

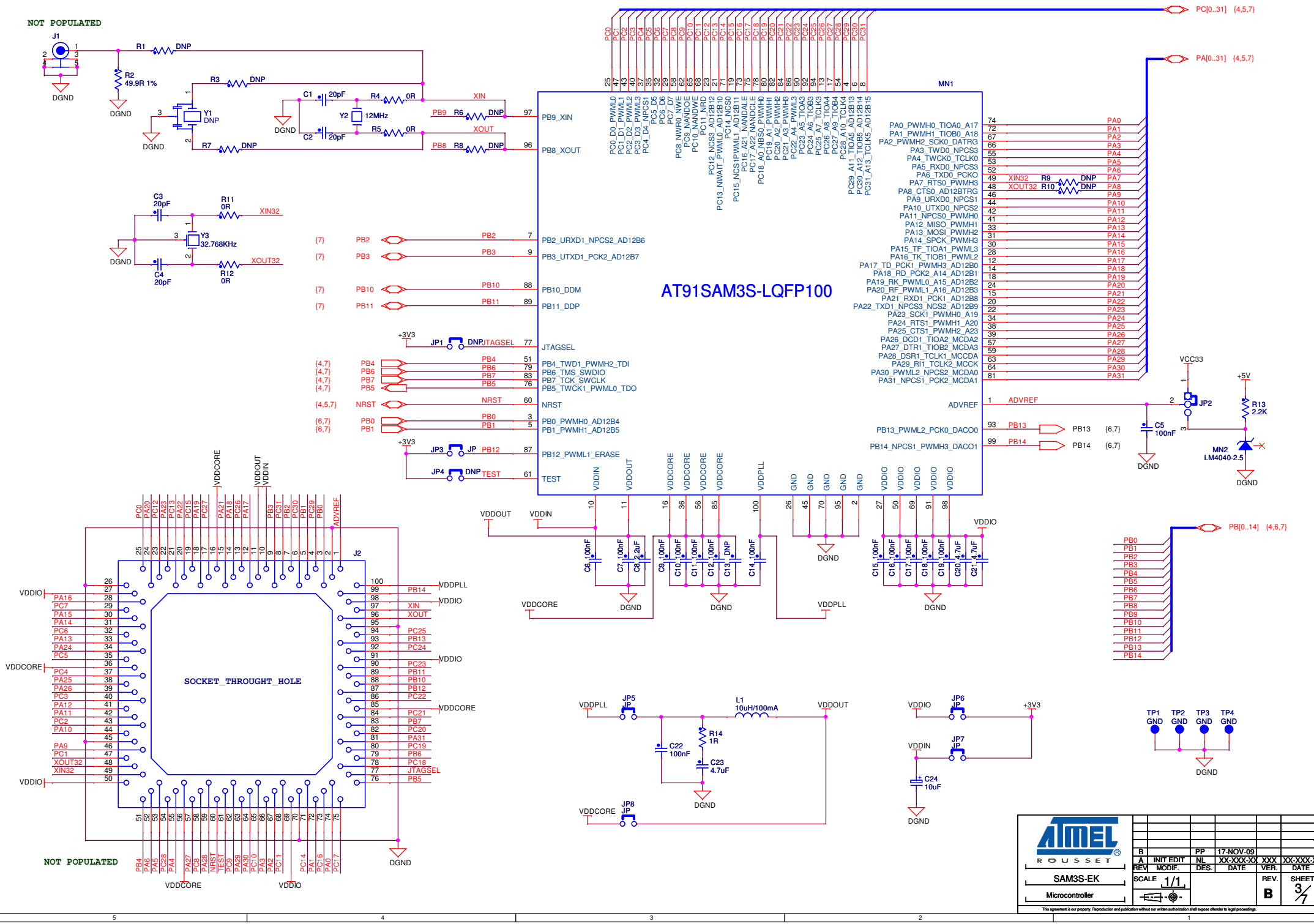
SAM3S-EK

Describe

SCALE 1/1

REV. B

SHEET 2/7


NOT POPULATED
J1
R1 DNP
R2 49.9R 1%
R3 DNP
R4 0R
R5 0R
R6 DNP
R7 DNP
R8 DNP
C1 20pF
C2 20pF
Y1 DNP
Y2 12MHz
XIN
XOUT
PB9
PB8
C3 20pF
C4 20pF
R11 0R
R12 0R
Y3 32.768KHz
XIN32
XOUT32
AT91SAM3S-LQFP100
MN1
PC[0..31] {4,5,7}
PA[0..31] {4,5,7}
PB[0..14] {4,6,7}
PB2_URXD1_NPCS2_AD12B6
PB3_UTXD1_PCK2_AD12B7
PB10_DDM
PB11_DDP
JTAGSEL
PB4_TWD1_PWMH2_TDI
PB6_TMS_SWDIO
PB7_TCK_SWCLK
PB5_TWCK1_PWML0_TDO
NRST
PB0_PWMH0_AD12B4
PB1_PWMH1_AD12B5
PB12_PWML1_ERASE
TEST
PB13_PWML2_PCK0_DACO0
PB14_NPCS1_PWMH3_DACO1
ADVREF
JP1 DNP JTAGSEL
JP3 JP PB12
JP4 DNP TEST
JP2
R13 2.2K
C5 100nF
MN2 LM4040-2.5
VCC33
+5V
+3V3
VDDIN
VDDOUT
VDDCORE
VDDPLL
VDDIO
GND
C6 100nF
C7 100nF
C8 2.2uF
C9 100nF
C10 100nF
C11 100nF
C12 100nF
C13 DNP
C14 100nF
C15 100nF
C16 100nF
C17 100nF
C18 100nF
C19 100nF
C20 4.7uF
C21 4.7uF
J2
SOCKET_THROUGHT_HOLE
NOT POPULATED
JP5 JP
L1 10uH/100mA
R14 1R
C22 100nF
C23 4.7uF
JP8 JP
JP6 JP
JP7 JP
C24 10uF
TP1 GND
TP2 GND
TP3 GND
TP4 GND
DGND
SAM3S-EK
Microcontroller
ROUSSET
B PP 17-NOV-09
A INIT EDIT NL XX-XXX-XX XXX XX-XXX-XX
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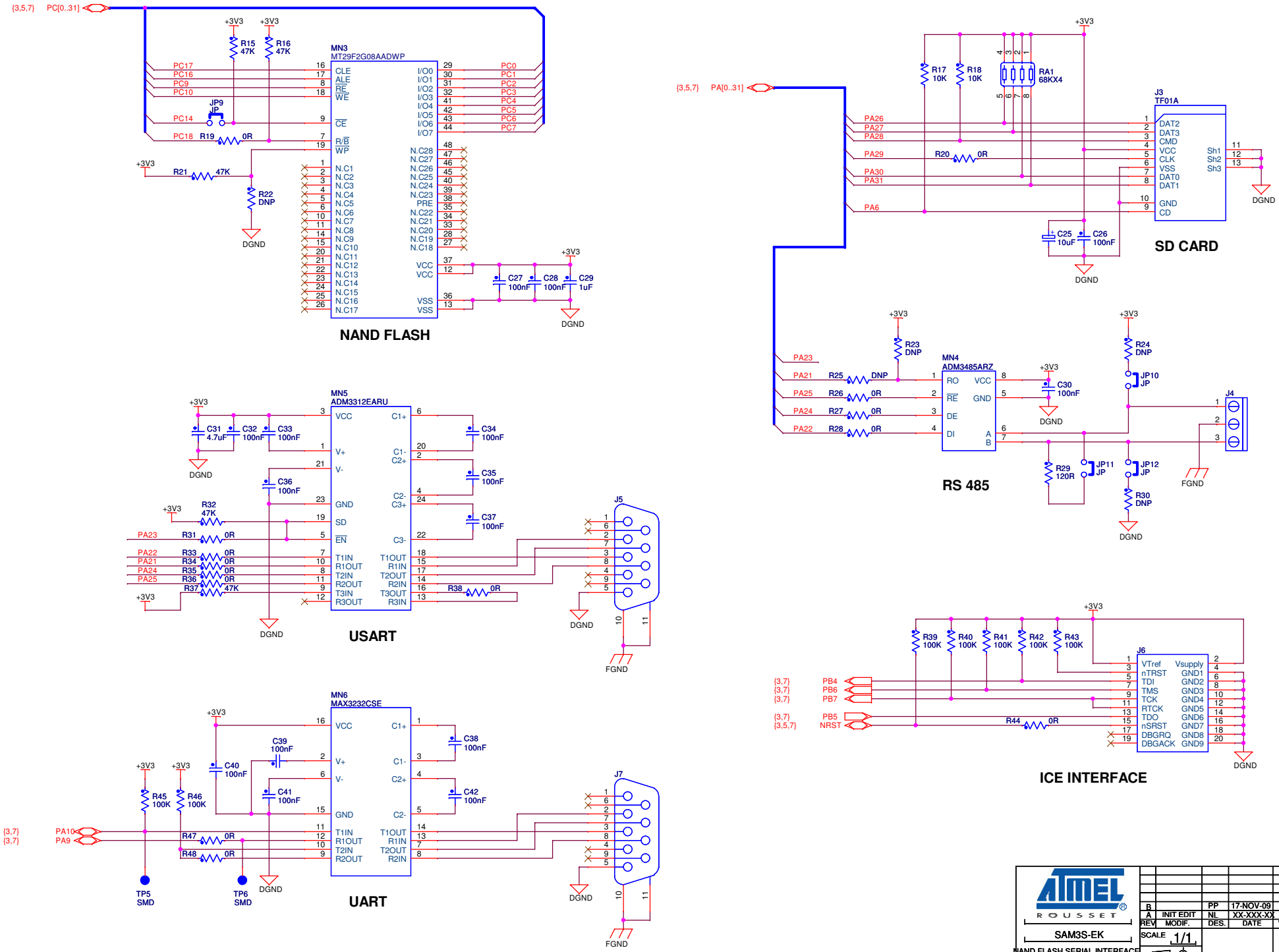
NAND FLASH
MN3
MT29F2G08AADWP
SD CARD
J3
TF01A
RS 485
MN4
ADM3485ARZ
USART
MN5
ADM3312EARU
UART
MN6
MAX3232CSE
ICE INTERFACE
J6
SAM3S-EK
NAND FLASH,SERIAL INTERFACE
ATMEL
ROUSSET
SCALE 1/1
REV. B
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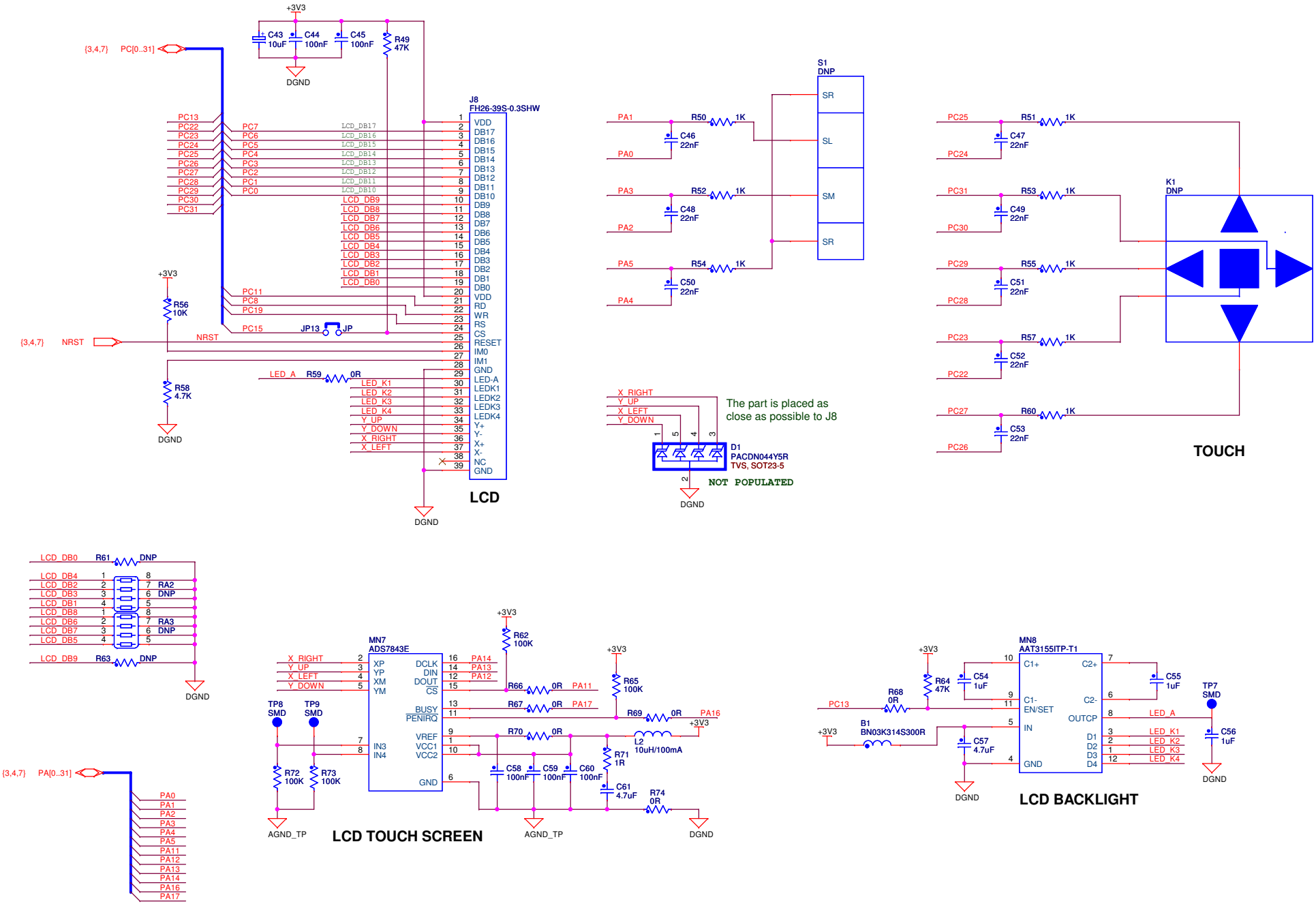
17-NOV-09



REV.	MODIF.	DES.	DATE	VER.	DATE
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SAM3S-EK

TFT-LCD & QTouch

SCALE 1/1

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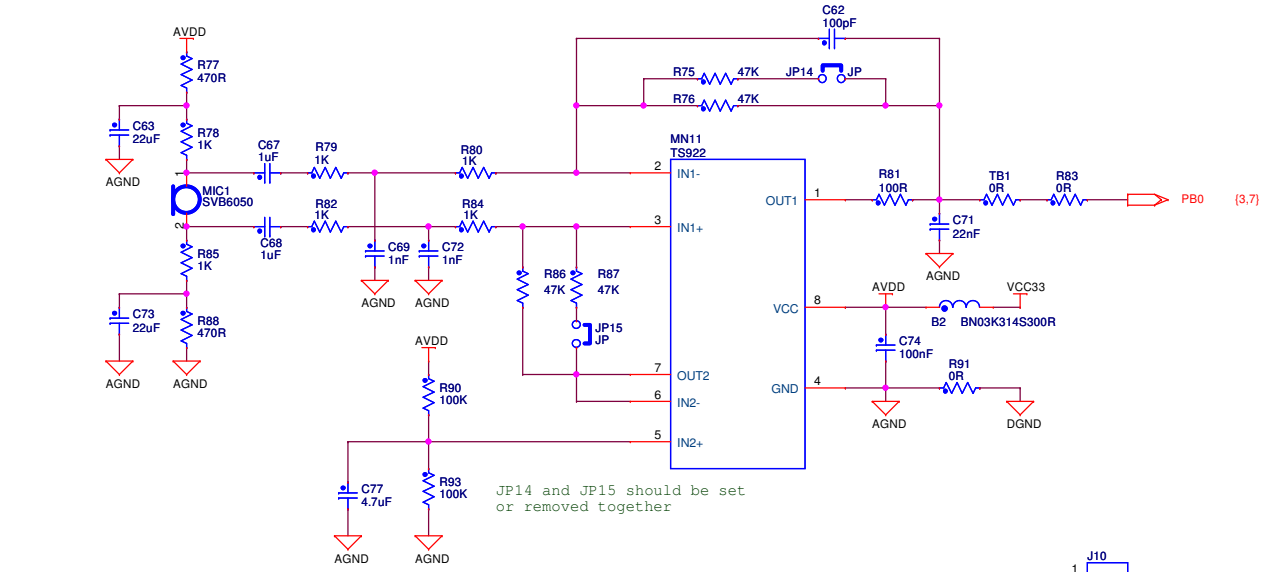
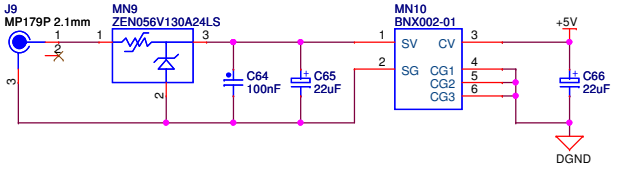
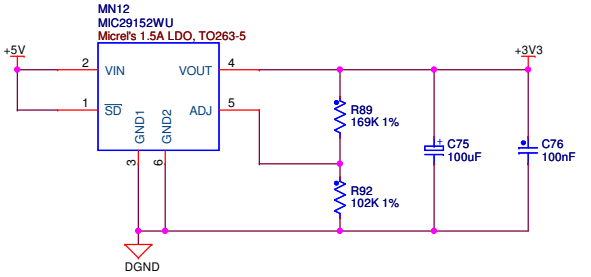
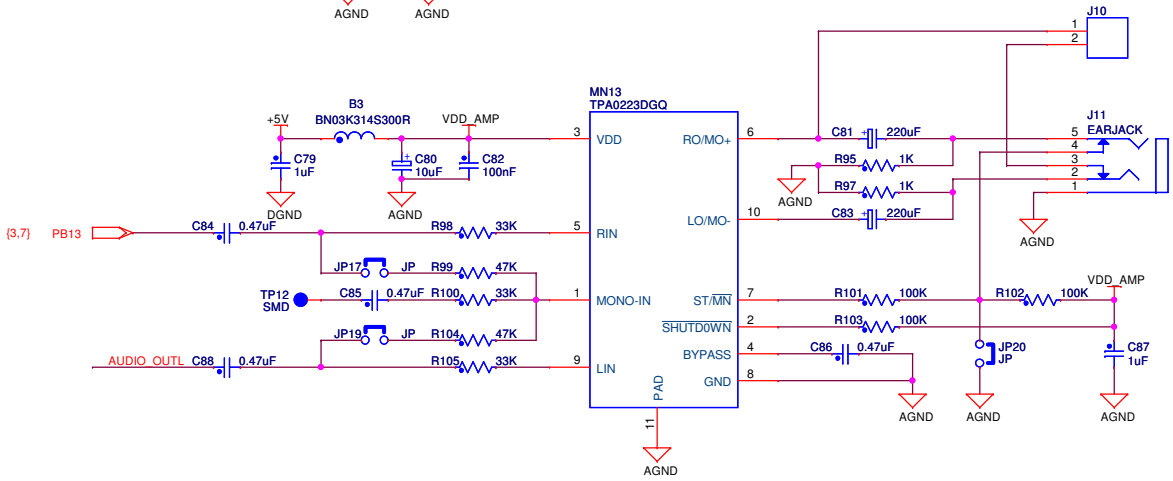
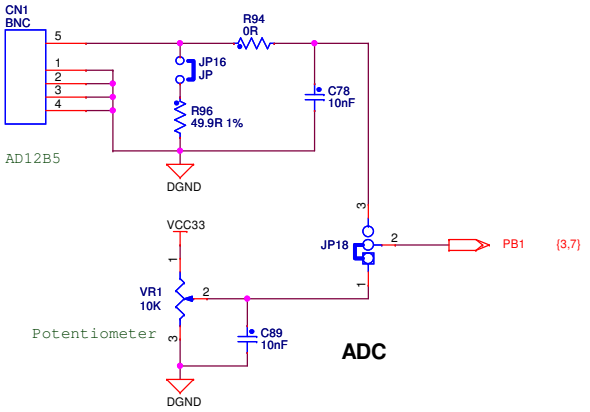
AUDIO IN



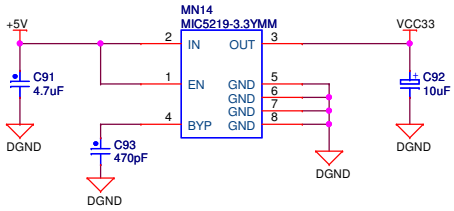


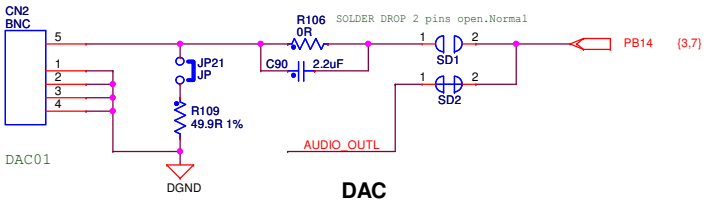






AUDIO OUT





B		PP	17-NOV-09			
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REV.	MODIF.	DES.	DATE	VER.	DATE	

SAM3S-EK

Audio & Power Supply

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REV. B

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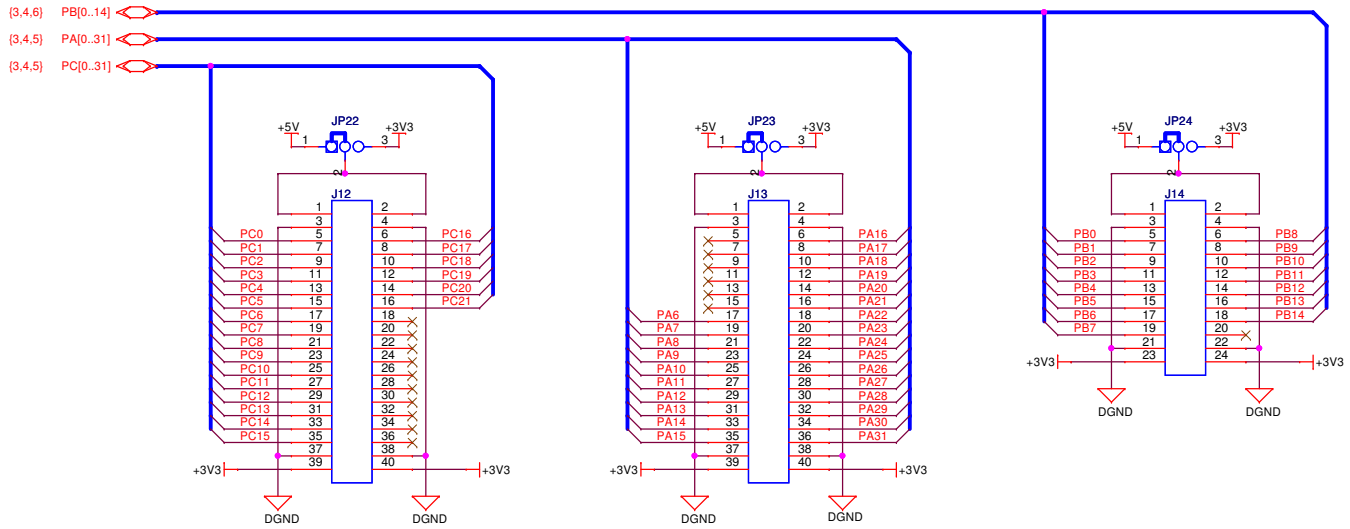
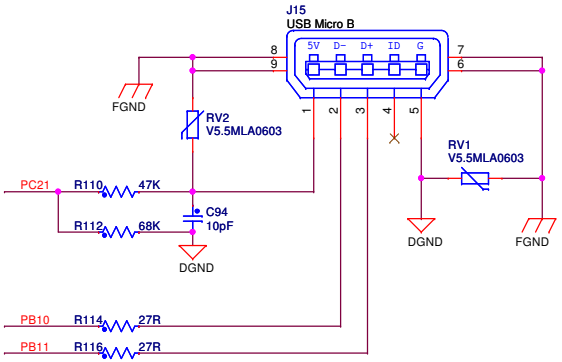
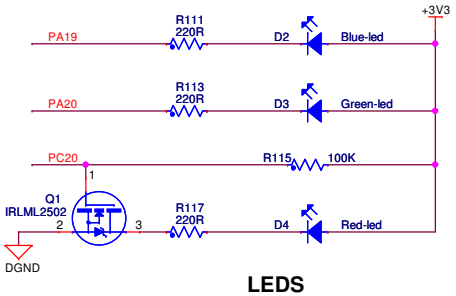


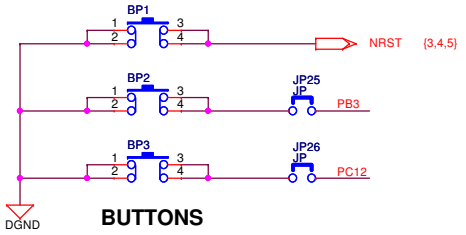
PIO EXPANSION



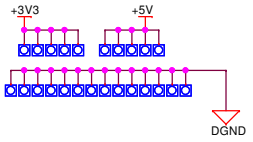
USB

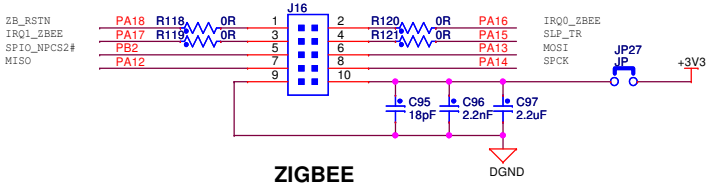


LEDS



BUTTONS





ZIGBEE

REV.	MODIF.	DES.	DATE	VER.	DATE
B		PP	17-NOV-09		
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SAM3S-EK

MISC

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